## REMARKS

Claims 17-35 are pending in this application. By this Amendment, claims 17, 19, 20, 23 and 26-30 are amended and claims 31-35 are added. The claim amendments and added claims introduce no new matter. A Request for Continued Examination is attached. Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Applicants appreciate the courtesies shown to Applicants' representative by Examiner Memula in the August 19, 2008 personal interview. Applicants' separate record of the substance of the interview is incorporated into the following remarks.

The Office Action, in paragraph 2, rejects claims 17-25 and 27 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 2002/0125933 to Tamura et al. (hereinafter "Tamura"). The Office Action, in paragraphs 14, 18, 22 and 26 rejects claims 26 and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Tamura in view of one or more of U.S. Patent Application Publication No. 2003/0222698 to Khieu et al. (hereinafter "Khieu"), U.S. Patent Application Publication No. 2004/0085120 to Pitts, U.S. Patent No. 5,594,261 to Temple, U.S. Patent No. 6,188,109 to Takahashi, U.S. Patent Application Publication No. 2002/0014880 to McAndrews, U.S. Patent Application Publication No. 2002/0014663 to Iwamatsu et al. (hereinafter "Iwamatsu"), U.S. Patent Application Publication No. 2004/0077151 to Bhattacharyya, U.S. Patent Application Publication No. 2004/0087084 to Hsieh, U.S. Patent Application Publication No. 2004/0094763 to Agnello et al. (hereinafter "Agnello"), and U.S. Patent Application Publication No. 2004/0018668 to Maszara. These rejections are respectfully traversed.

Claim 17 recites, among other features, a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising a first and a second electrical supply terminal and

a clock input, the subassemblies being connected in series by means of their supply terminals to the terminals of a voltage supply source, wherein a same clock signal is applied to the clock input of all subassemblies, by means of a device for shifting the levels of the clock signal, and wherein the subassemblies are formed in such a way that the same current flows through each of the subassemblies. Tamura, even in combination with any of the other applied references, cannot reasonably be considered to teach, to have suggested or to have provided any reason to make, this combination of features for at least the following reasons.

Tamura teaches a driver circuit for correctly transmitting signals at high speed without waveform distortion, the driver circuit including an output driver, a front driver, and a level adjuster, the front driver driving the output driver, and the level adjuster adjusting the output level of the front driver (Abstract). With reference to Fig. 8, the Office Action alleges that the embodiment depicted in Fig. 8 includes several features that correspond to those recited in claim 17, as quoted above. The Office Action, however, relies on at least a separate and distinct embodiment of the front driver 4 of Tamura as allegedly being combinable, in some manner, with the embodiment of Fig. 8, asserting that this combination of embodiments teaches features that correspond to feature wherein a same clock signal is applied to the clock input of all subassemblies by a device for shifting the levels of the clock signal, as is recited, among other features, in independent claim 17. The analysis of the Office Action fails in at least this regard for the following reasons.

With reference to Fig. 2, Tamura states, at paragraph [0123], "[a] driver circuit shown in Fig. 2 has an output driver 1, a front driver 4, and a level adjuster 5 and is connected to a receiver 2 through a signal transmission line 3." Tamura indicates that the driver circuit of the first aspect shown in Fig. 2 is characterized by a combination of the level adjuster 5 and front driver 4 for compensating attenuations of high-frequency components in the

transmission line 3 (see paragraph [0124]).. The combination of the level adjuster 5 and the front driver 4 is indicated as modifying an input signal SS to generate a signal S1.

In order to find the feature of a plurality of transistors connected to one another so as to form a plurality of functional elements, as is recited, among other features, in independent claim 17, the Office Action references Fig. 8, elements 44-47. The Office Action asserts that this series of four functional elements is grouped in subassemblies, each comprising a first and a second electrical supply terminal and a clock input as is positively recited, among other features, in independent claim 17. The Office Action then asserts that the feature wherein a same clock signal is applied to the clock input of all subassemblies by means of a device for shifting the levels of the clock signals is shown in a combination of Fig. 8 with some combination of Figs. 1, 2 and 7.

It should be noted that Fig. 1 is indicated as a driver circuit for transmitting signals according to the prior art (paragraph [0019]). No level adjustment of any kind is depicted in Fig. 1. As indicated above, Fig. 2 depicts a broad overview of the device disclosed in Tamura in which a front driver 4 and a level adjuster 5 are provided. At paragraphs [0144] - [0145], Fig. 8 is described as depicting a front driver 4 of a driver circuit for transmitting signals according to the third embodiment of the first aspect of the present invention. The front driver 4, in Fig. 8, is formed as a current limiting inverter consisting of PMOS transistors and NMOS transistors that are connected in series. The SS signal is commonly applied to the gates of certain of the transistors, while the gates of other transistors receive control voltages Vcp and Vcn. In this regard, although not depicted in Fig. 8, the control terminals receive inputs Vcp and Vcn from a level adjuster, so that the signal output from front driver 4 is level adjusted based on these inputs when signal SS changes digitally from 0 to 1 or 1 to 0.

The analysis of the Office Action asserts that a same clock signal SS is applied to the clock input of all subassemblies by means of a device for shifting the levels of the clock

signal. According to Fig. 8, signal SS is directly connected to transistors 44 and 47. No device for shifting levels of the signal SS is used. The Office Action refers to Figs. 1, 2 and 7. For the reasons noted above, reference to Figs. 1 and 2 is not pertinent. Further, with respect to Fig. 7, Tamura states that the level adjuster 5 and the front driver 4 emphasize the high frequency component of an input signal SS to generate signal S1. In this regard, level adjustment occurs to vary the output level of the front driver. The level adjuster 5 modifies signal SS to vary the level of signal S1.

Fig. 12 provides further insight into the level adjustment that occurs in the front driver 4 according to Fig. 8. As is described in paragraph [0156] of Tamura, the front driver 4 depicted in Fig. 12 "is the same as that of FIG. 8". The level adjuster 5 is shown as controlling voltage generator 55 for generating control voltages Vcp and Vcn according to a current provided internal to the level adjuster 5 shown in Fig. 12. As such, it is clear that any level adjustment that occurs in a front driver 4 configured as shown in Figs. 8 and 12 occurs based on adjustment of Vcn and Vcp and not by shifting any level of any clock signal input to the allegedly corresponding plurality of subassemblies.

Further, the description of Fig. 7, at paragraphs [0140] - [0143] in Tamura, shows a front driver 4 that consists of an amplifier 41, a variable gain unit 42, and a feedback resistor 43. The Office Action appears to allege, and, as was clarified during the August 19 personal interview with Examiner Memula, is intended to assert that the embodiment of Fig. 7 can somehow be inserted in the SS line leading to the embodiment shown in Fig. 8. Examiner Memula specifically referred to paragraph [0389] of Tamura for an assertion that different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. The Examiner relies on this assertion as supporting the proposition that the differing embodiments of Figs. 7 and 8 are combinable in some manner. However, each of Figs. 7 and 8 discloses a distinct and independent construction of a front

driver 4 of separate embodiments. These embodiments are not combinable in the manner asserted by the Office Action. Each of the depicted embodiments drives the input SS signal providing level adjustment within the device such that an output S1 signal is level adjusted via different and exclusive methodologies and structures.

At the interview, Examiner Memula argued that the SS signal input of front driver 4 depicted in Fig. 8 "could be" level adjusted by the front driver 4 in Fig. 7 prior to being introduced to the front driver 4 in Fig. 8. Such a reading requires that Tamura be construed as teaching sequential front drivers 4 of differing configurations for sequential modification of the signals passing through them, which is clearly not explicitly, or impliedly, disclosed in Tamura. Further, each of Figs. 7 and 8 depicts a specific construction of the front driver 4. With reference to Fig. 2, there is no basis by which to assert that the Tamura device may include separate and distinct front drivers 4 in series for separately level adjusting signal inputs in some manner.

Based on the above, there is no basis by which to assert that Tamura teaches any feature that can reasonably be considered to correspond to "a same clock signal is applied to the clock input of all subassemblies by means of a device for shifting the levels of the clock signal," as is positively recited, among other features, in independent claim 17. Clearly, although Tamura teaches that some embodiments may be available for some combination of features disclosed, combining elements of differing embodiments of the front driver 4 as are separately disclosed in Figs. 7 and 8 is impermissible.

In reviewing the anticipation standard, the Federal Circuit has stated "[t]o anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375 (Fed. Cir. 2001), *cert. denied*, 122 S. Ct. 1436 (2002). Additionally, other court precedent clarifies the requirements for anticipation stating that "the reference ... must clearly and

unequivocally disclose the claimed compound or direct those skilled in the art to the compound without any need for picking, choosing and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkley*, 455 F.2d 586, 587, 172 USPQ 524 (CCPA 1972); *see also Sandisk Corp. v. Lexar Media, Inc.*, 91 F. Supp. 2d 1327, 1336 (N.D. Cal. 2000) (stating that "[u]nless all the elements are found in a single piece of prior art in exactly the same situation and united the same way to perform the identical function, there is no anticipation") and *Aero Industries Inc. v. John Donovan Enterprises-Florida Inc.*, 53 USPQ2d 1547, 1555 (S. D. Ind. 1999) (stating that "[n]ot only must a prior patent or publication contain all of the claimed elements of the patent claim being challenged, but they 'must be arranged as in the patented device'"). This standard for anticipation is also set forth in MPEP §2131, which states that "the identical invention must be shown in as much detail as is contained in the ... claim." Further, although the same terminology need not be used, "the elements must be arranged as required by the claim."

The Office Action improperly ignores these requirements for anticipation by modifying the embodiment of Fig. 8 of Tamura to introduce an unrelated level adjustment of Fig. 7 of Tamura to attempt to render anticipated the subject matter of the pending claims. In this regard, the Office Action improperly "picks and chooses" elements from distinct embodiments in attempting to show that the combination of all the features positively recited in independent claim 17 is taught by the Tamura reference.

Also, because any level adjustment that occurs in Tamura occurs as the input signal is processed through the front driver 4, it is unreasonable to assert that Fig. 7 provides any teaching regarding the same clock signal applied to the clock input of all subassemblies occurring "by a device for shifting levels of the clock signal."

Finally, it should be noted that one of ordinary skill in the art would not have modified the Tamura device to include sequential drivers in that it is unclear based on any disclosure of

Tamura what any output signal from such a combination would look like. Additionally, it is unclear what utility any such signal may have. In this regard, Tamura discloses a very detailed scheme for modifying an input signal SS to provide an output signal S1 based on some level adjustment in the front driver 4 the Tamura device. To modify such a signal via the front driver of Fig. 7, and then to subsequently modify the output of the front driver of Fig. 7 with the front driver of Fig. 8 (see also Fig. 12) would yield a signal that would likely not resemble the input SS signal in any meaningful way.

None of Khieu, Pitts, Takahashi, McAndrews, Iwamatsu, Bhattacharyya, Hsieh, Agnello and Maszara, in any combination with Tamura overcome the shortfalls in the application of Tamura to the combination of all of the features recited in claim 17, as discussed above. Additionally, claims 18-30 are neither taught, nor would they have been suggested by, the applied references for at least the respective dependence of these claims on allowable claim 17, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of 17-30 under 35 U.S.C. §§102 and 103 are respectfully requested.

Claims 31-35 recite other patentably distinct features. These claims are also neither taught, nor would they have been suggested, by the applied references for at least the respective dependence of these claims on allowable claim 17, as well as for the separately patentable subject matter that each of these claims recites.

The added claims are directed to features specifically achievable by the disclosed device. These claims recite features that limit the structure of the device recited in claim 17. There is no manner by which Tamura can reasonably be considered to teach features such as those recited in claims 31-35. For example, Tamura fails to teach any feature wherein the subassemblies are formed in such a way that the same current flows through each of the

subassemblies as positively recited in independent claim 17. Claim 34 is added to clarify that the subassemblies are formed in such a way that, at all times in operation, the same current flows through each of the subassemblies. Claim 35 recites a similar feature. This feature is clearly not taught by the Tamura reference. This is just one example of the additional features recited in the added claims that is not taught by the Tamura reference. Careful review of the features recited in each of the added claims reveals that these features, in addition to the features argued above regarding claim 17, cannot reasonably be considered to be taught by the Tamura reference.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 17-35 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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WPB:DAT/sld

Attachments:
Request for Continued Examination
Petition for Extension of Time

Date: August 25, 2008

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